Single Carrier Communication System on Open Source Embedded Platform

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Abstract— *Modern open source embedded platforms are very cost effective while providing enormous computing power. Open source embedded platforms with processor clock frequency exceeding 1GHz speed are common and ideal for implementing Digital Communication Transceivers using Software Radio concept. Many of the open source embedded platforms are equipped with an Analog to Digital Converter (ADC) allowing sampling signals exceeding 1MHz rate. This allows implementing Encrypted Digital Data Services using a Software Radio concept. In this work we have modelled in Matlab Simulink environment, major functions of a Single Carrier Baseband Digital Transceiver, including Pulse Shaping, Carrier Modulation, Timing Recovery, Carrier Recovery, Matched Filtering and Data recovery using, BPSK, QPSK and QAM modulation schemes. The equalization function is not implemented as this is intended for Line of Sight Microwave and Satellite applications where the need for equalization is limited. The Pulse shaping is performed using Gaussian Pulse Shaping. Timing recovery is carried out using Gardner's Algorithm based technique and Carrier Recovery is implemented using a Costas Loop and its variants implemented in software. A prototypes for BPSK, QPSK and QAM modulation schemes were implemented in MATLAB Simulink environment and BPSK modulation scheme is implemented in an Arduino-Due micro controller using Arduino Development Environment. The proof of concept in this work shows the potential of software radio in off the shelf embedded hardware.*

Keywords—**BPSK, QPSK, QAM, DSP, Matlab, Simulink, Timing Recovery, Carrier Recovery**

I. INTRODUCTION

Single Carrier Communication has a long history in the Digital Communication Receivers and whether they are inferior to their counterpart Multi Carrier Systems is debatable even today. Using Non-linear frequency domain equalization using widely available FFT hardware allow Single Carrier Communication Systems to have the same implementation advantages of Multi-carrier systems to stay as a competitive candidate. Single carrier systems use a single channel to transmit a broadband signal using data pulses of shorter duration resulting a wideband spectrum susceptible to frequency selective fading. However non-linear equalization allows these channel impairments to be rectified to give performance and simplicity advantage over Multi-Carrier systems. Therefore in communication applications where direct Line of Sight (LOS) channel is available with insignificant Multi-path interference, single carrier communication is attractive due to its simplicity, spectral efficiency and less memory demanding nature in implementation. Direct Microwave Links and Digital Data modulated streams for satellite communication are potential applications of single carrier systems. Timing synchronisation in single carrier systems are less memory hungry compared to Multi carrier Systems. In OFDM multi carrier system one OFDM symbol worth of data has to be stored internally to perform Cyclic-Prefix correlation to implement timing synchronisation. Even other functions are in the transceiver chain of a single carrier system work sample by sample basis and therefore less memory demanding. This makes single carrier systems to be attractive for implementing on the embedded hardware as a software radio concept.

II. METHODOLOGY AND EXPERIMENTAL DESIGN

A. Transmitter

Transmitter converts binary bit stream into a baseband carrier modulated signal. Carrier modulated broadband signal is then transmitted through wireless channel. In this work, baseband carrier modulated signal is transmitted in a wired medium to avoid radio frequency transmission. The implemented transmitter functions are as follows.

1) Bit stream generation: The Transmitter functionality is modelled by generating a continuous pseudo-random unipolar bit stream.

2) Unipolar to Bipolar conversion: Created unipolar bit stream then was converted to bipolar bit stream to represent the baseband Binary Phase Shift Keying (BPSK) data.

3) Reduction of transmission bandwidth: This bipolar binary data is then converted into a sampled data stream

of Gaussian shape pulses to reduce the transmission bandwidth. This was achieved by multiplying the rectangular bit samples by a Gaussian shaped pulse stored in a look-up table. This simpler approach for Pulse Shaping gives a compromise between theoretical rigour of pulse shaping and simplicity in implementation.[1] The sharpened edge of pulses get converted into Gaussian dumbbell shape reducing the required transmission bandwidth while minimizing interference to adjacent channels.

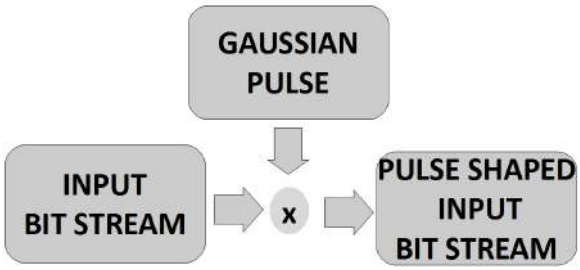

Figure 1. Blocked diagram of pulse shaping using Gaussian pulse

*4) Modulation: T*he Gaussian pulse shaped bit stream are then multiplied by the baseband carrier signal internally generated to be synchronous with the data signal. The carrier frequency is chosen to be ten times the data rate. The modulation scheme and the transmitted symbol determines the starting phase of the carrier. Subsequent up-conversion into an RF carrier (if needed) would increase the carrier frequency as required. QPSK system is modelled by appropriately changing the starting phase of the carrier signal at the start of the data pulse with four possible starting phases separated by 90^{o} in the constellation diagram of input data symbols. In QAM system, both Amplitude and the Phase of the Data signal are varied according to the constellation of the data symbol being transmitted.

The carrier modulated QAM signal is constructed by using Quadrature Carriers modulated with appropriate In-phase and Quadrature data of QAM signal. This prototype implementation does not perform RF carrier modulation. The transmitted signal generated with the Baseband Carrier is used as the receiver input.

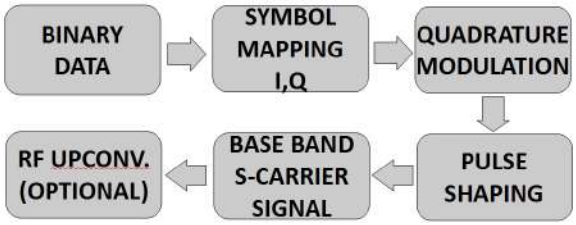

Figure 2. Single Carrier Transmitter Block Diagram

B. Receiver

At the receiver the baseband carrier modulated signal is converted to its baseband data signal. The carrier recovery, timing recovery and matched filtering is performed at the receiver for signal synchronization and optimum noise free detection.

1) Analog to Digital Conversion: The Receiver samples the baseband carrier modulated signal using the Analog to Digital Converter (ADC) in the embedded platform. The sampling rate set to nominal value of the transmitter sampling rate. The nominal sampling interval is adjusted to be early or late with respect to the regular sampling point by using the timing error generated by the Gardner's algorithm implemented using the baseband data signal recovered later in the receiver chain. [3]

2) Timing recovery: The timing error correction compensates for slight frequency mismatch in transmitter and receiver crystal oscillators to stop possible data loss due to accumulated timing error. Timing error corrected signal is then processed for carrier recovery using Costas-Loop, which consists of a Phase Locked Loop that recovers the baseband BPSK data. For QPSK and QAM a slight variation of Costas-Loop is being used. [2] This recovered data down sampled to have two samples per bit to be used in the Gardner's Algorithm for timing recovery at the front-end ADC.

3) Carrier recovery and demodulation: The Costas-loop recovers the baseband carrier while giving out the demodulated signal.

4) Match filtering: The match-filter is placed within the costas-loop carrier recovery scheme. The matched filter eliminates the out of band noise of the baseband signal. This helps the optimum detection of received signal bits.

C. Costas Loop

The costas loop performs both phase coherent suppressed carrier reconstruction and synchronous data detection within the loop.

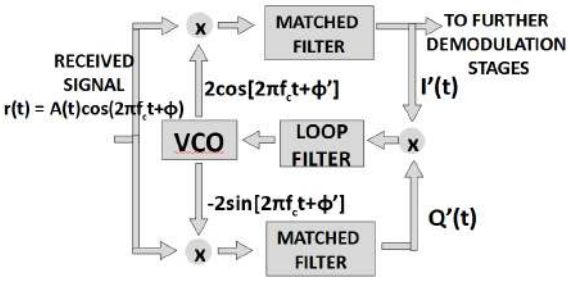

Figure 3. Block Diagram of the Costas Loop BPSK modulation scheme

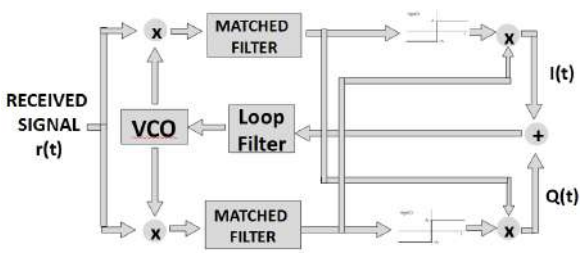

Figure 4. Block Diagram of the Costas Loop QPSK and QAM modulation scheme

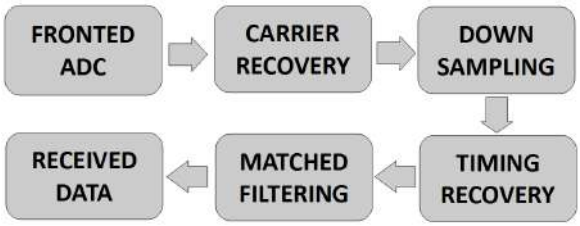

Figure 5. Single Carrier Receiver Block Diagram

Costas loop functionality is based on the orthogonally of sin [Θ (t)] and cos [Θ (t)] functions.
A signal of the form A(t) cos (2*pi*ft+φ) only contains power in the in-phase component. The received signal r (t) can therefore be described as:

$$(t)=I(t)\cos(2\pi fct+\emptyset)+Q(t)\sin(2\pi fct+\emptyset)$$

Where I(t) =1 and Q(t) =0 (BPSK). In practice the VCO is never perfectly synchronized with the carrier therefore both arms of the Costas loop receive some of the signal power as given by the following equation,

$$I'(t)=A(t)\cos(\emptyset-\emptyset')$$
$$Q'(t)=A(t)\sin(\emptyset-\emptyset')$$

In a Costas loop the input to the loop filter is the product of these two signals.

$$e(t)=A^2(t)\cos(\emptyset-\emptyset')\sin(\emptyset-\emptyset')$$
$$=0.5A^2\sin(2(\emptyset-\emptyset'))$$

$$e(t)=0.5A^2(t)\sin(2(\emptyset-\emptyset'))$$

Where (φ- φ') is the phase mismatch between the received carrier and local VCO carrier. The loop filter then removes any nose which comes from the term $A^2(t)$ so that the VCO produces a stable recovered carrier for demodulation.

D. Timing Recovery

The receiver never knows the precise bit interval of the pulses as transmitter clock can be slightly offset from the nominal value due to practical reasons. The receiver must know where to take the samples within each symbol interval for the continuous bit stream with no accumulated timing error to eventually slip off bits. Timing recovery consists estimation timing error using Gardner's Algorithm and appropriately offsetting the sampling interval to eliminate the timing error.

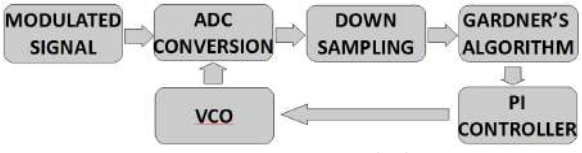

Figure 6. Timing recovery Block Diagram

Gardner's Algorithm:

Timing Error = $e_n= (Y_n-Y_{n-2})Y_{n-1}$

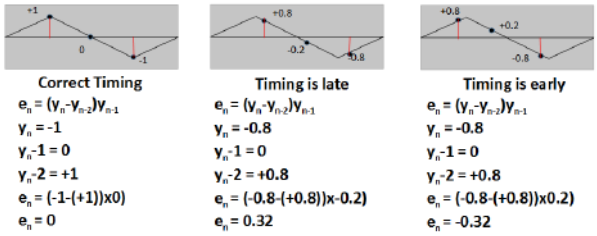

Figure 7. Gardner's algorithm demonstration for correct timing, late timing and early timing

e_n = 0, no timing adjustment is required for the next symbol
$e_n > 0$, a timing advanced is required for the next symbol
$e_n < 0$, a timing delay is required for the next symbol

Time spacing between Y_n and Y_{n-2} is T seconds.
Time spacing between Y_n and Y_{n-1} is T/2 seconds.

III. RESULTS AND DISCUSSION

MATLAB Simulink models were implemented for BPSK, QPSK and QAM modulation schemes. These models were very useful in implementing the transceiver in real time embedded system. The PID and filter parameters of the system were determined using the Simulink model. The BPSK modulation scheme based transmitter and receiver was implemented on Arduino Due embedded platform that runs on a 80MHz clock. The software model proved that a data signal can be received by eliminating any timing error or carrier error present in the signal before implementation in real embedded hardware. The embedded software was prototyped in Matlab to verify the correctness of the algorithms before implementation. Carrier recovery and Timing recovery were implemented and tested separately and subsequently integrated to make the complete working prototype. The receiver input signal had some noise mixed during the signal transmission through the wired channel. BPSK transceiver implementation was successful in the embedded hardware. QPSK and QAM implementations are more sensitive to recovered carrier phase and implementation on embedded hardware needs further improvements. The possible effects of slight timing jitter in real-time implementation of a communication system in microcontroller based system compared to dedicated hardware implementation is to be investigated. These aspects will be looked into in the future work.

IV. CONCLUSION

This project has proved the feasibility of implementation of a single carrier communication system as a software radio concept in embedded hardware. The Gaussian pulse shaping, elimination of Timing error and carrier synchronization error were demonstrated in simulation and real-time hardware. The Gardner's algorithm was

used to eliminate the timing error and Costas-loop based carrier recovery method were implemented completely in software. BPSK, QPSK and QAM modulation schemes were implemented in MATLAB Simulink environment and BPSK modulation scheme is implemented in an Arduino-Due micro controller using Arduino Development Environment. Relatively low rate digital transceiver implementation on open source embedded hardware shows potential of low cost solutions in Early warning systems, Internet of Things (IOT) and sensor networks.

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